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REUSED VLSI ARCHITECTURE OF CHANNEL ENCODING USING SOLS TECHNIQUE FOR DSRC APPLICATIONS

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ABSTRACT

The dedicated short-range communication (DSRC) is an originating technique to puts the step forward ofintelligent transportation system into our daily routine life. The DSRC standards generally acceptFM0 and Manchester codes to reach dc-balance and enhances the signal reliability. Oftenly, the differentially of coding betweenthe FM0 and Manchester codes predominantly limits the potential to design a fully reused VLSI architecture for both. In this paper, we are introducing term the similarity-oriented logic simplification (SOLS) technique. The maximum operation frequency is 2 GHz and 900 MHz for Manchester and FM0encodings, respectively. The power consumption take place is 1.58 mW at2 GHz for Manchester encoding and 1.14 mW at 900 MHz forFM0 encoding. The core circuit area is 65.98 × 30.43 µm.The encoding simplicity and capability of this paper can fully support or acceptable by the any DSRC standards. This paper not only develops a fully reused VLSI architecture, but also exhibits an efficient performance as compared with the existing works.

Keywords: *Dedicated short-range communication (DSRC), FM0, Manchester, VLSI.*

I. INTRODUCTION

The dedicated short-range communication (DSRC)is nothing but the protocol for one- or two-way medium or short range communication. This DSRC can be classified into two categories automobile-to-automobile and automobile-to-roadside. In automobile-to-automobile, the DSRC processes the message sending and broadcasting among automobiles for the sake of safety issues and public information announcement.

In The safety issues include blind-spot, intersection warning, inter cars distance, and collision-alarm. The automobile-to-roadside focuses on the intelligent transportation service, such as electronic toll collection (ETC) system. With ETC, the toll collecting is electrically accomplished with the contactless IC-card platform.

Moreover, the ETC can be extended to the payment for parking-service, and gas-refueling. Thus, the DSRC system plays an important role in modern automobile industry.

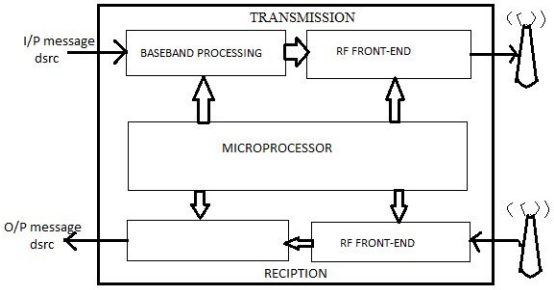

Fig:1

The system architecture of DSRC transceiver is shown in Fig. 1. The upper and bottom parts are dedicated for transmission and receiving, respectively. This transceiver is classified into three basic modules: microprocessor, baseband processing, and RF front-end. The microprocessor interprets instructions from media access control to schedule the tasks of baseband processing and RF front-end. The baseband processing is responsible for modulation, error correction, clock synchronization, and encoding. The RF frontend transmits and receives the wireless signal through the antenna.

The DSRC standards have been established by several organizations in different countries. These DSRC standards of America, Europe, and Japan are shown in Table I.

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TABLE I
PROFILE OF DSRC STANDARDS FOR AMERICA, EUROPE, AND JAPAN

	Europe	America	Japan
Organization	CEN[1]	ASTM[2]	ARIB[3]
Data Rate	500 kbps	27 Mbps	4 Mbps
Carrier Frequency	5.8 GHz	5.9 GHz	5.8 GHz
Modulation	ASK, PSK	OFDM	ASK
Encoding (Downlink)	FM0	Manchester	Manchester

[1] European Committee for Standardization.
[2] American Society for Testing and Materials.
[3] Association of Radio Industries and Businesses.

The DSRC standards have been established by several organizations in different countries. These DSRC standards of America, Europe, and Japan are shown in Table I. The data rate individually targets at 500 kb/s, 4 Mb/s, and 27 Mb/s with carrier frequency of 5.8 and 5.9 GHz. The modulation methods incorporate amplitude shift keying, phase shift keying, and orthogonal frequency division multiplexing. Generally, the waveform of transmitted signal is expected to have zero mean for robustness issue, and this is also referred to as dc-balance. The transmitted signal consists of arbitrary binary sequence, which is difficult to obtain dc-balance. The purposes of FM0 and Manchester codes can provide the transmitted signal with dc-balance. Both FM0 and Manchester codes are widely adopted in encoding for downlink.

II. LITERATURE SURVEY

P. Benabes, A. Gauthier, and J. Oksman have proposed the system which consist of the processing of only Manchester encoding technique. And they proposed a VLSI architecture of Manchester encoder for optical communications. This design Exhibits the CMOS inverter and the gated inverter as the switch to construct Manchester encoder for better security. It is implemented by 0.35-μm CMOS technology which has the operated frequency is of 1 GHz.

A. Karagounis, A. Polyzos, B. Kotsos, and N. Assimakis have replaced the architecture of switch and instead of that they used the nMOS device for the architecture of the VLSI and were able to increase the performance in terms of operating frequency. The operating frequency of this architecture was minimum 2.4GHz to maximum 5GHz.

Y.-C. Hung, M.-M.Kuo, C.-K.Tung, and S.-H. Shieh developed the high-speed VLSI architecture which was most likely closed to reused architecture by using the Manchester and Miller encoding technique. This architecture was used to design chips by the 0.35-μm CMOS technology. The maximum operating frequency of this architecture was 200 MHz.

M. A. Khan, M. Sharma, and P. R. Brahmanandha also proposed a FM0 encoding architecture
For the applications ultrahigh frequency (UHF) RFID tag emulator. This hardware architecture is based on the finite state machine (FSM) concept of Manchester's code. And also fist time used to implement on the field-programmable gate array (FPGA) prototyping system. The maximum operation frequency of this design is about 256 MHz.

Yu-Hsuan Lee and Cheng-Wei Pan have proposed the efficient, high-speed fully reused VLSI architecture with the help of combination of FM0 and Manchester encoding. The architectural design has reduced BER and used for the applications such small area communication.

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III. FEATURES OF THIS PAPER

Even though, we are proposing two channel encoding techniques at a time in this project to minimizes the BER and architectural area, the coding diversities between these two FM0 and Manchester practically limits the capacity to design an efficient and fully reused VLSI architecture with each other.

So the main concept of this project is to create a such architecture which reduces the area of the application circuit. The technique which we are going to use is nothing but the Similarity Oriented Logic Simplification, in which it sort out the similar part of the program of both techniques FMO and MANCHESTER and thus required architecture is to proposed for the common part of the both techniques and remaining individual encoding of both techniques.

Similarity-Oriented Logic Simplification (SOLS) technique is nothing but using similar logic commonly in multiple modules to reduce chip are. The SOLS consists of two core methods: 1) Area-Compact Retiming:

The area-compact retiming can be elaborated as it re allocates the hardware structure resources to reduce number of transistors which automatically reduces the number of hardware and archtectrual area.

2) Balanced Logic-Operation Sharing:

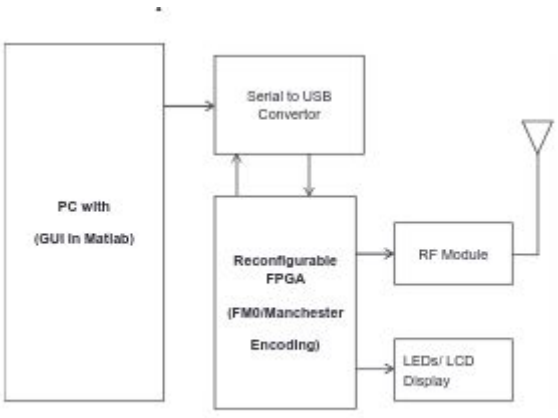
The balanced logic-operation sharing efficiently combines FM0 and Manchester encodings with the fully reused hardware architecture, which means the only architechture repeatedly used for the function of both encodings. Which results in the compact and small VLSI design.

IV. SYSTEM ACHITECTURE

The System architecture defines the whole control logic of transmission and receiving section for the DSRC application. Our proposed system is as shown in above fig. it contains two main parts transmitter and receiver.

As we are using these encoding methods for short range communication we will show some real time application of communication like transmission of text file from one pc to other PC. The role of PC in our project will be generation of random binary message or loading data file and transmitting that file on serial port as well as receiving processed data on serial port by FPGA.
We have to show some graphical analysis of communication like graph of SNR vs BER, for this we will use Matlab Software, where we can easily Create GUI based application on which we can show graphical analysis effectively.

Transmission part:



Here in the above figure we have shown the block diagram of transmission side of the architecture for DSRC application.

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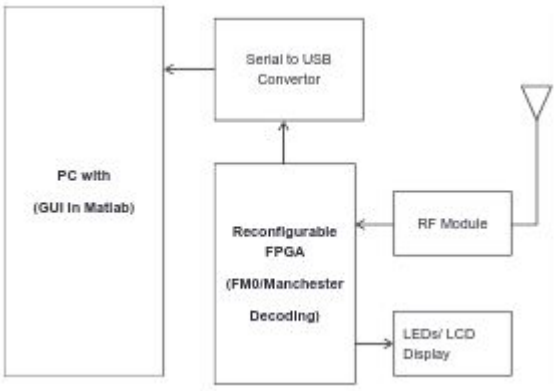
Receiving part:



This is the receiving part of the architecture for DSRC application. As we observe simply the both transmission and block are much similar. And used similar components also.

The VLSI architecture algorithm steps for DSRC application system generation are:
1) Start
2) Generate Radom Binary Data or
Get file from User.
3) Transmit Binary Data on Serial Port.
4) Receive Data on FPGA by serial protocol.
5) Encode Binary Data using FM0 or Manchester Encoding.
6) Transmit Data using RF Module.
7) Receive Data using Receiver side RF Module.
8) Decode Data using Same Method used at Transmitter side.
9) Send Decoded Data to PC on Serial Port.
10) Calculate BER between Transmitted and received Binary Data.
11) Visualize Graph of BER.
12) Stop.

HARDWARE EQUIPMENSTS:
A. FPGA (Spartan 6)

B. Serial to USB Convertor

C. RF Modules

D. LED/ Switches

E. PCB

F. Computer/Laptop

A. FPGA (SPARTAN 6):

Mimas is the name of this FPGA tool processor; it is easy to use FPGA development board featuring Xilinx Spartan-6 FPGA. Mimas is specially designed for experimenting and learning system design with FPGAs. It is a computer architecture combining some of the flexibility of software with the high performance of hardware by processing with very flexible high speed computing fabrics like field-programmable gate arrays (FPGAs).

The principal difference when compared to using ordinary microprocessors is the ability to make substantial changes to the data path itself in addition to the control flow. On the other hand, the main difference with custom hardware, i.e. application-specific integrated circuits (ASICs) is the possibility to adapt the hardware during runtime by loading a new circuit on the reconfigurable fabric.

The main task of FM0 and Manchester Encoding will be performed on FPGA. To make architecture area efficient we will try to use part of similar logical circuit of FM0 and Manchester commonly using SOLS method.

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FPGA is the main processing part of this project or we can say it is the heart of this project. Because it decides the architecture for the two encoding techniques FMO and Manchester. This part controls the flow of the data and whole programmed work. The whole flow of this projected is to be first coded in the software (Xilinx and Matlab) and then it is to be dumped on this FPGA processor kit. High-Performance Reconfigurable Computing (HPRC) is a computer architecture combining reconfigurable computing-based accelerators like FPGAs with CPUs or multi-core microprocessors.

B. SERIAL TO USB CONVERTOR

A USB adapter is a type of protocol converter which is used for converting USB data signals to and from other communications standards. Commonly, USB adaptors are used to convert USB data to standard serial port data and vice versa. As most of latest PC or Laptops doesn't contain serial port we have to Serial to USB Converter. Most commonly the USB data signals are converted to either RS232, RS485, RS422 or TTL serial data. The older serial RS423 protocol is rarely used any more, so USB to RS423 adapters are less common.

The on board full speed USB controller helps a PC/Linux/Mac computer to communicate with this module. Use a USB A to Mini B cable to connect with a PC. By default the module is powered from USB so make sure not to overcrowd unpowered USB hubs. (The picture on the left shows USB Mini connector).

C. RF Modules

As we are proposing this scheme for Dedicated Short Range Communication (DSRC) we can use any short range communication protocol like WiFi, Bluetooth as well as RF. In our Project we are going to use RF transmitters and Receivers for short range communication upto 10 meter range.

An RF module (radio frequency module) is a (usually) small electronic device used to transmit and/or receive radio signals between two devices. In an embedded system it is often desirable to communicate with another device wirelessly. This wireless communication may be accomplished through optical communication or through radio frequency (RF) communication.

RF modules are most often used in medium and low volume products for consumer applications such as garage door openers, wireless alarm systems, industrial remote controls, smart sensor applications, and wireless home automation systems. They are sometimes used to replace older infra red communication designs as they have the advantage of not requiring line-of-sight operation. Several carrier frequencies are commonly used in commercially-available RF modules, including those in the industrial, scientific and medical (ISM) radio bands such as 433.92 MHz, 915 MHz, and 2400 MHz. These frequencies are used because of national and international regulations governing the used of radio for communication. Short Range Devices may also use frequencies available for unlicensed such as 315 MHz and 868 MHz. RF modules may comply with a defined protocol for RF communications such as Zigbee, Bluetooth low energy, or Wi-Fi, or they may implement a proprietary protocol.

D. LED/ Switches

LEDs and Switches are used for testing purposes whether we are getting or sending the exact data or some mismatch is there in the user window of transmitting on the PC or laptop. LEDs and Switches are mounted on the FPGA tool kit for the easy of understanding.

E. PCB

Printed Circuit Board are used for the mounting of varies components and devices on the electronic board for the convenient transmission of the data and power flow and easy to handle the device or product.

F. COMPUTER/LAPTOP

This one is for the user. In this project, we are going to use two PCs at both of the ends transmitter and receiver end as shown in the above diagrams. We are making one type of Graphical User Interface (GUI) on the PC or Laptop which makes the user more reliable and very convenient toward the product.

G. SECURITY REQUIREMENTS

The results of our analysis are the following security requirements, which describe the background of our security framework. First the execution of any data is based on its context. We have to focus on the security functions of the desired design module. There are varies methods to track the data in the form of malware. Security has the prime importance in our project.

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V. SECURITY FEATURES

In any of the communication terminology there is the risk of the data malware and hacking of the data. Keeping this thing in mind we have concentrated here on security of data and provided a safty by the channel encoding techniques which mainly reduces the errors and provides an endurable security and authentication.

The FMO and MANCHESTER encoding and decoding techniques demonstrates forward correction and automatic repeat request which provides phenomenal authentication, encryption and decryption.

VI. EXPERIMENTAL RESULTS

I have represented the experimental results and explain the feasibility of my proposed solution. In my experimental setting, whether FM0 or Manchester code is adopted, no logic component of the proposed VLSI architecture is wasted. Every component is active in both FM0 and Manchester encodings. Therefore, the HUR of the proposed
VLSI architecture is greatly improved.

The logic functions of SOLS technique can be realized by various logic families. Each logic family optimizes one or more electrical performance, such as area, power, or speed, from circuit topology perspective instead of architecture perspective. The proposed SOLS technique is developed from architecture perspective to achieve 100% HUR. Among the logic families, both static CMOS circuit and transmission gate logic are widely applied in digital circuit owing to the operation frequency of Manchester encoding. Suppose its operation frequency can be scaled up to 2 GHz by 5.14 times and so does its power consumption, which is 1.44 mW at 2 GHz. Overall operation frequency and power consumptions is rated as 2.4 GHz to 5 GHz at the rate of 2mW of the power consumption.

VII. FUTURE SCOPE

There are tremendous works for the future which we can extend to our project. In this, we are doing half duplex communication and in the next work extend to full duplex communication system. As it seems this system is based on the VLSI architecture it also be categorized in the RFID applications. Now we are transferring data over limited range but for the future applications its range can be increased replacing particular types of RF modules.
Currently we are working on textual notice board system by sending the text, but furthermore it can be extend to transmit an audio notices with the help of some audio hardware like mic and speakers.

VIII. CONCLUSION

The coding-diversity between FM0 and Manchester encodings causes the limitation on hardware utilization of VLSI architecture design. A limitation analysis on hardware utilization of FM0 and Manchester encodings is discussed in detail. In this paper, the fully reused VLSI architecture using
SOLS technique for both FM0 and Manchester encodings is proposed. The SOLS technique eliminates the limitation on hardware utilization by two core techniques: area compact retiming and balance logic-operation sharing.

The area-compact retiming relocates the hardware resource to reduce 22 transistors. The balance logic-operation sharing efficiently combines FM0 and Manchester encodings with the identical logic components. The maximum operation frequency is 2 GHz and 900 MHz for Manchester and FM0 encodings, respectively. The power consumption is in range of 2 mW at 2 GHz for Manchester encoding and 1.5mW at 900 MHz for FM0 encoding. The encoding capability of this paper can fully support the DSRC standards for different applications. This paper not only develops a fully reused VLSI architecture, but also exhibits a competitive performance compared with the existing works.

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